The Architects View Framework: A Modeling Environment for Architectural Exploration and HW/SW Partitioning

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12.10.2004

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Outline

- Transaction Level Modeling Overview
  - Problem Statement
  - MP-SoC Design Flow
  - Terminology and Standardization: The 4 TLM Views
- Architects View Framework
  - Virtual Architecture Mapping technology
  - Tooling

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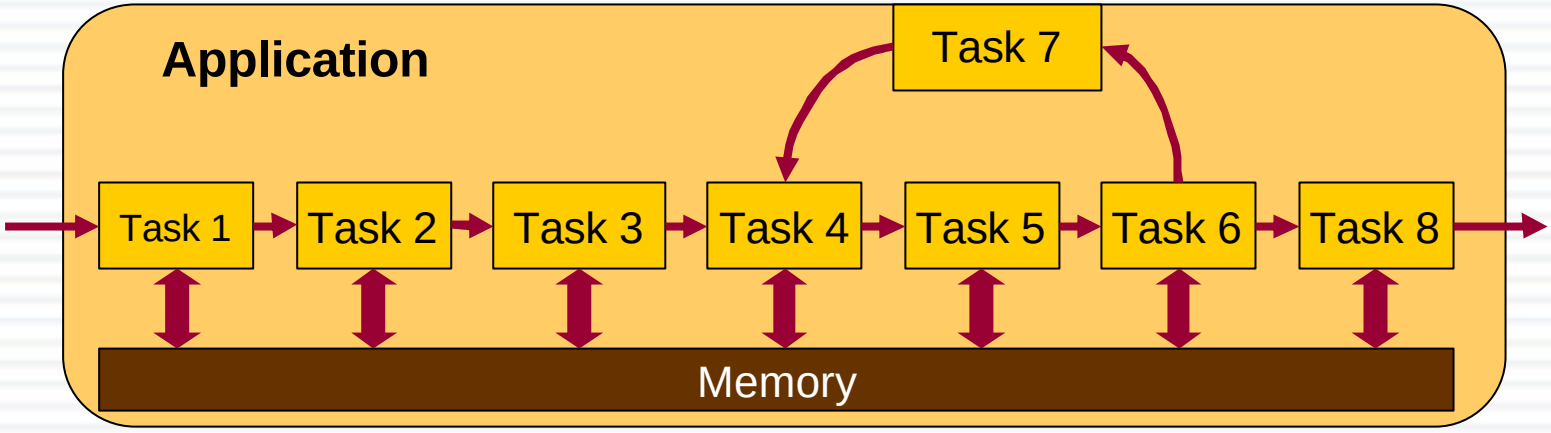
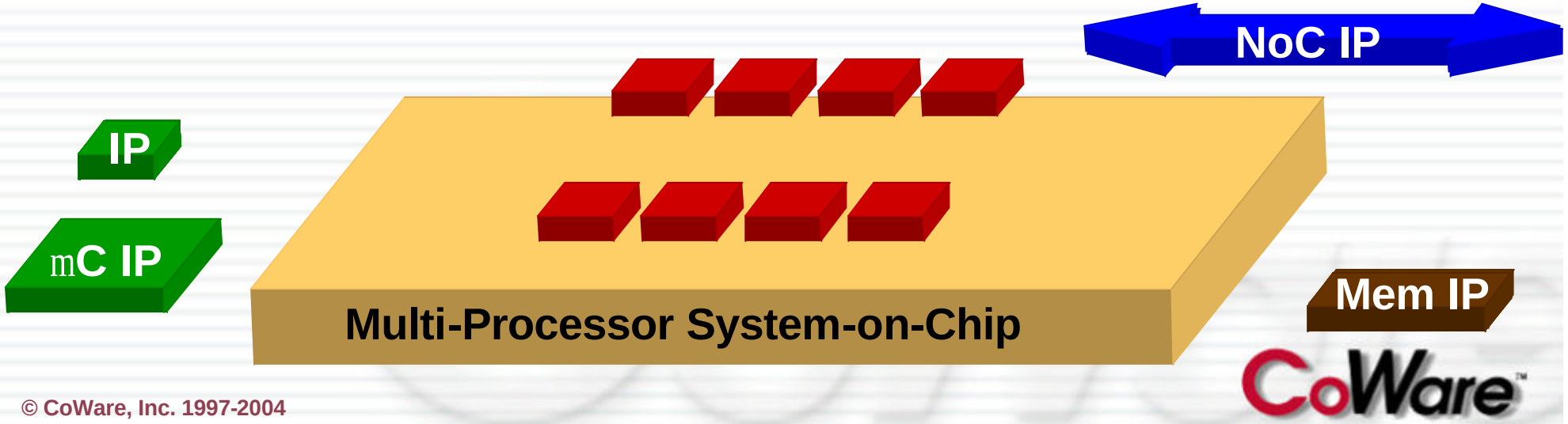
MP-SoC Platform Design Challenge



Spatial & Temporal Mapping



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Multi-level SoC Design

Magarshak/Paulin, DAC03

- System application design
  - domain specific algorithm design
  - eSW design
- MP-SoC platform design
  - specification, assembly and configuration of existing IP
  - spatial & temporal mapping of application to MP-SoC platform
  - eSW verification and profiling
  - reference model for HW verification

TLM domain

- High-level IP block design
  - embedded Processors: RISC, DSP, ASIPs
  - interconnect: busses, NoC
  - standard I/O: PCI, SPIx, DDR/QDR, …
- Technology & basic IP
  - memories
  - heterogeneous technologies: eDRAM, eFLASH, RF, ...

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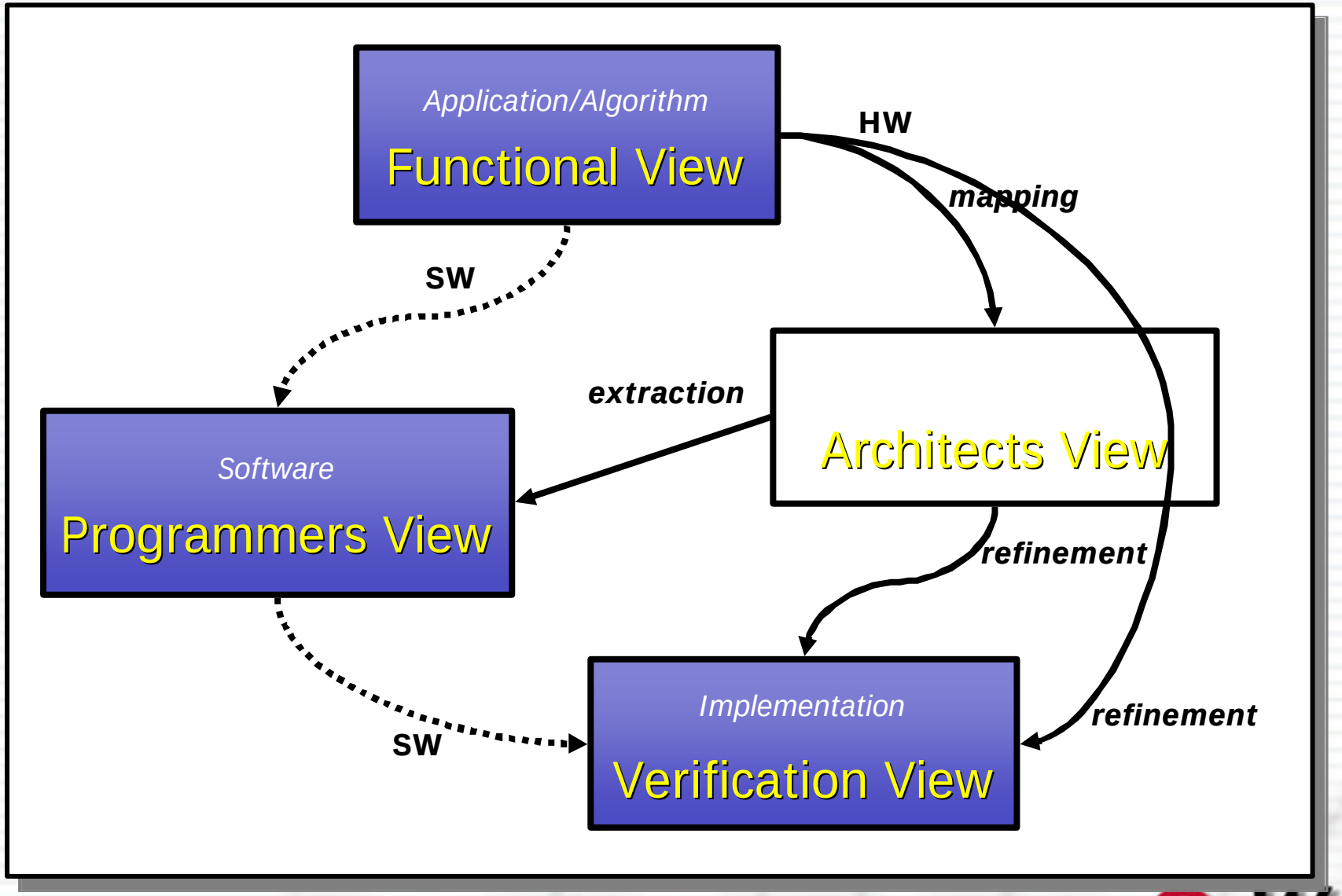
TLM based MP-SoC design flow



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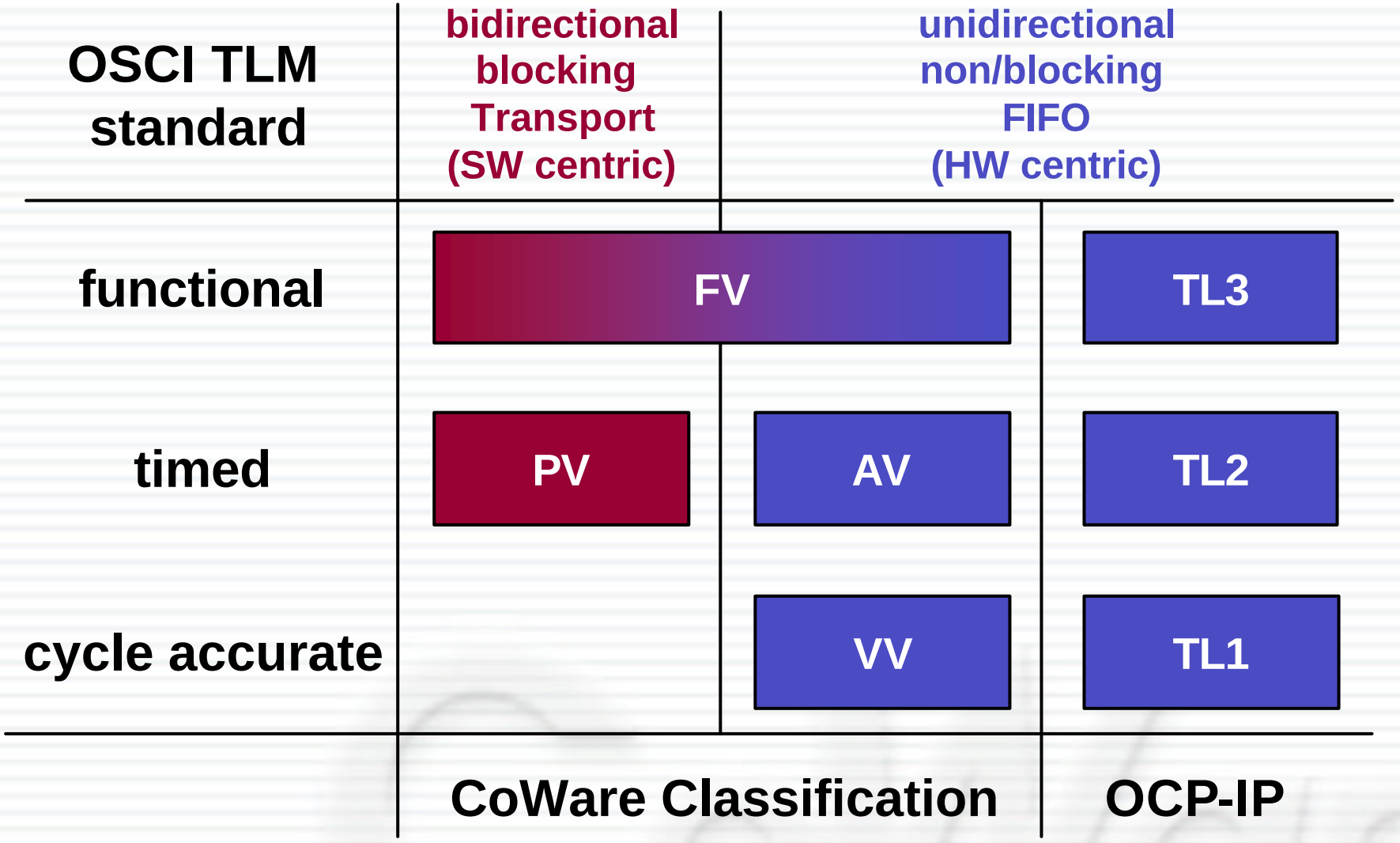
TLM Standardization Matrix



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  - Workflow
  - Virtual Architecture Mapping technology
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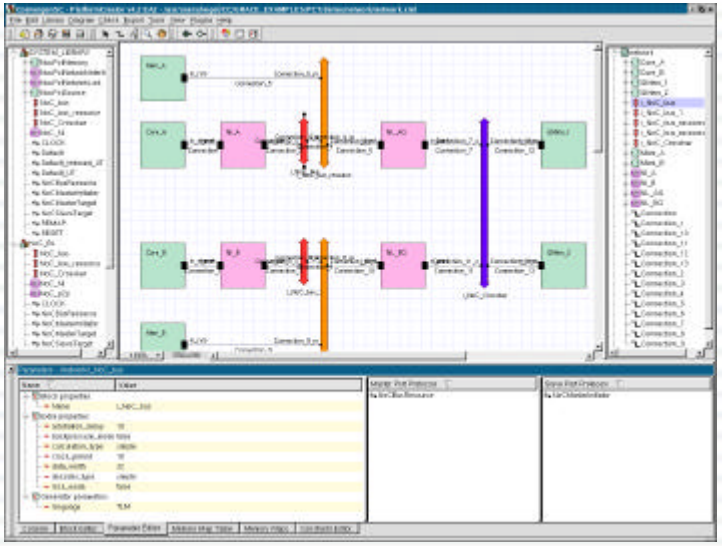
Architects View Framework

User Models

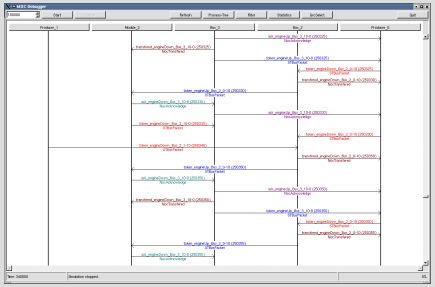
Architecture Models

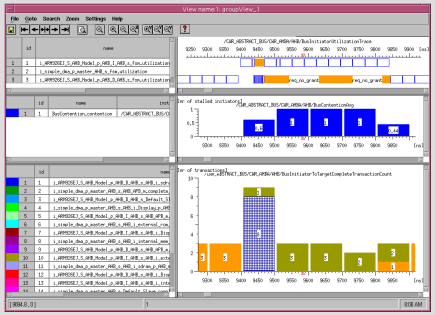


configuration files

SystemC Simulation

simulation results





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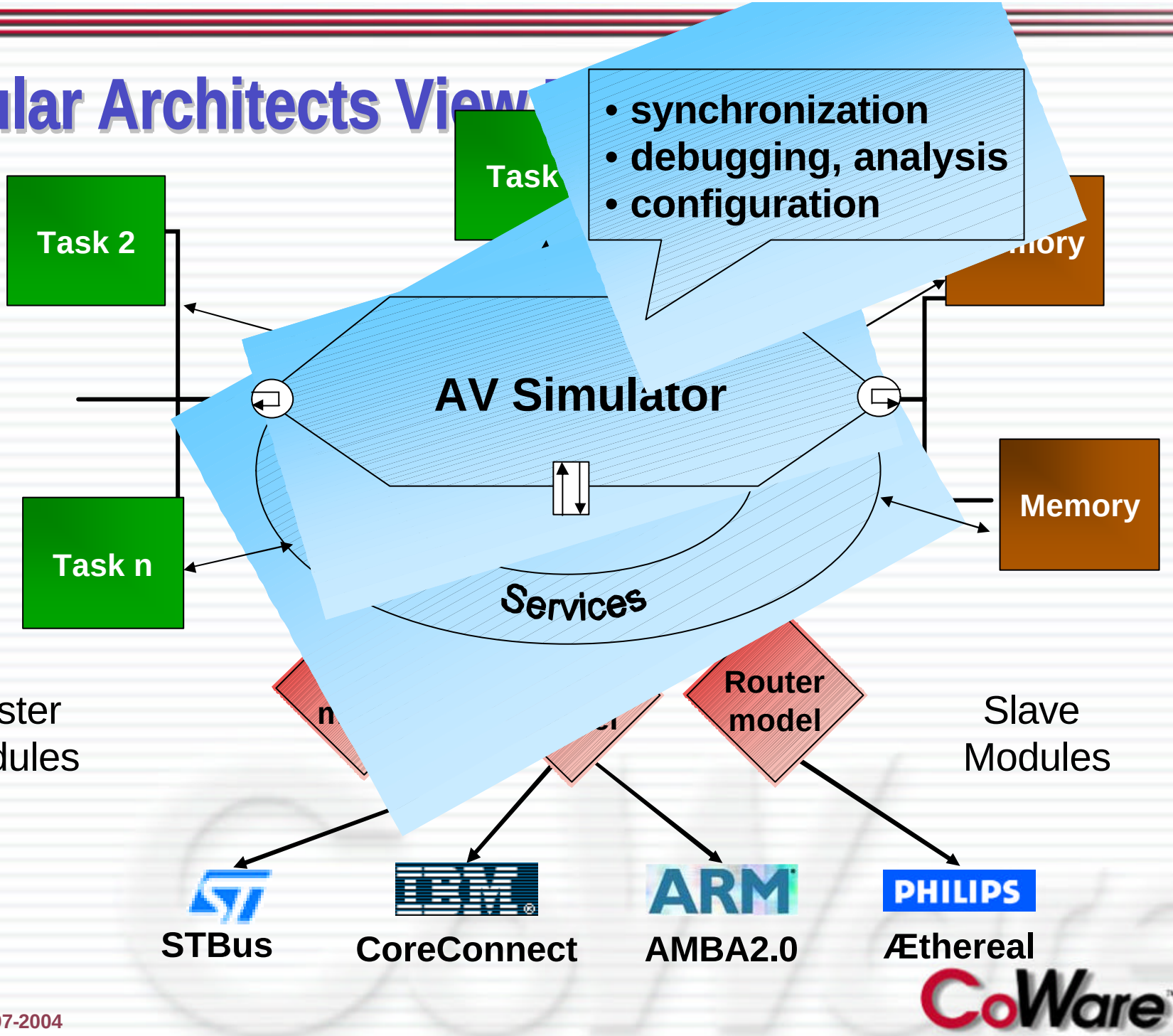
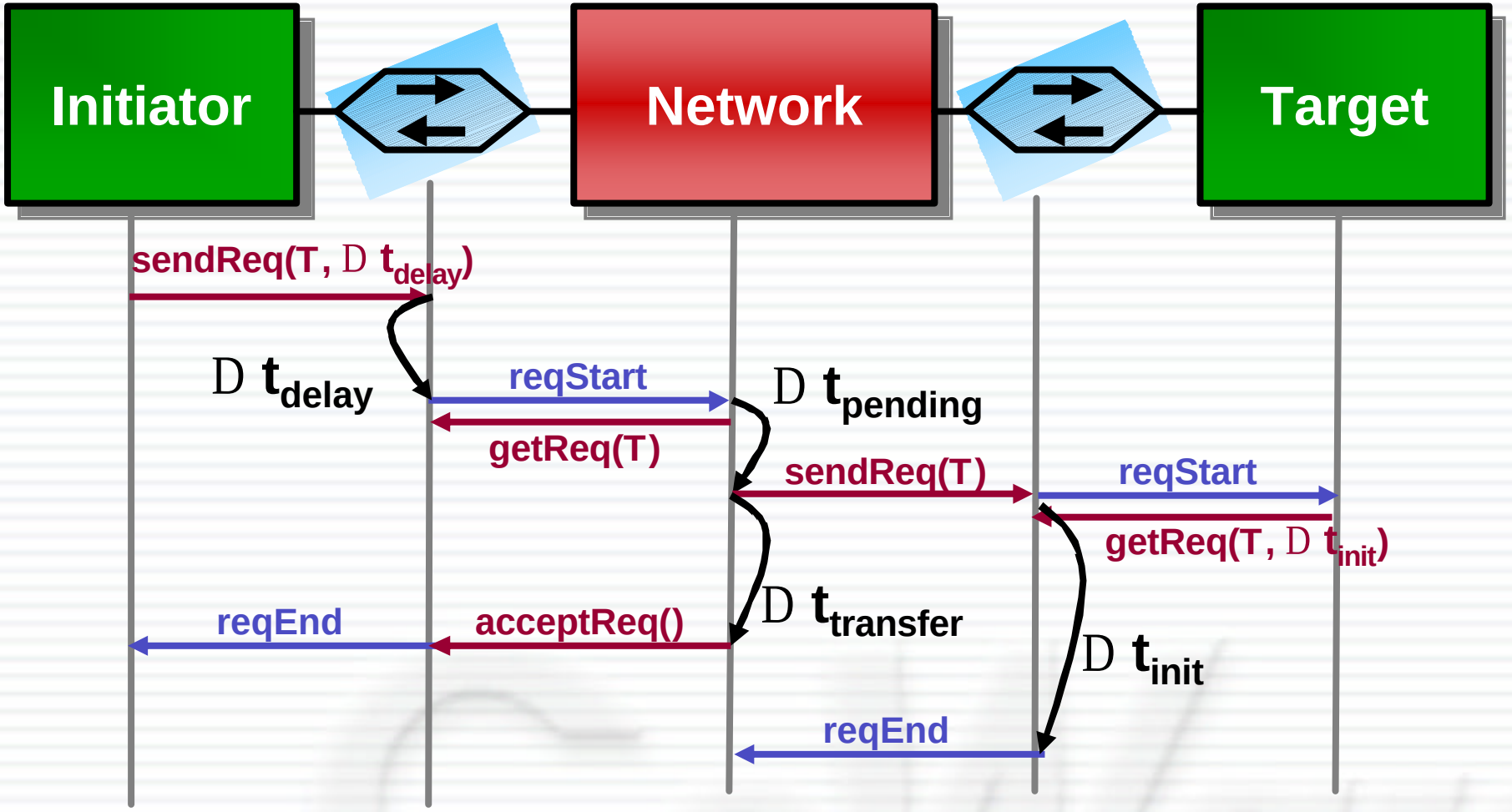
Modular Architects View



Implicit Timing Annotation



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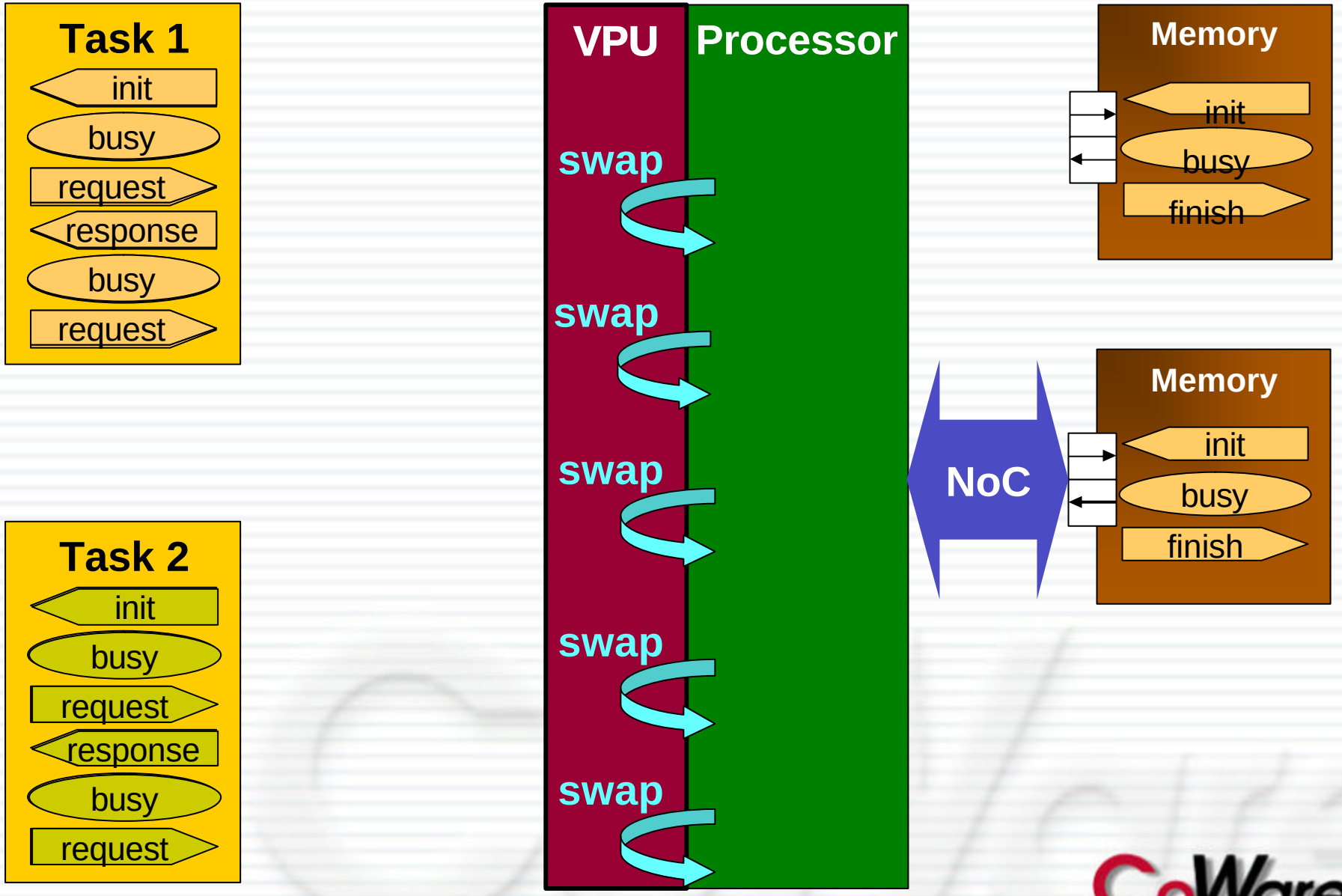
Virtual Processing Unit



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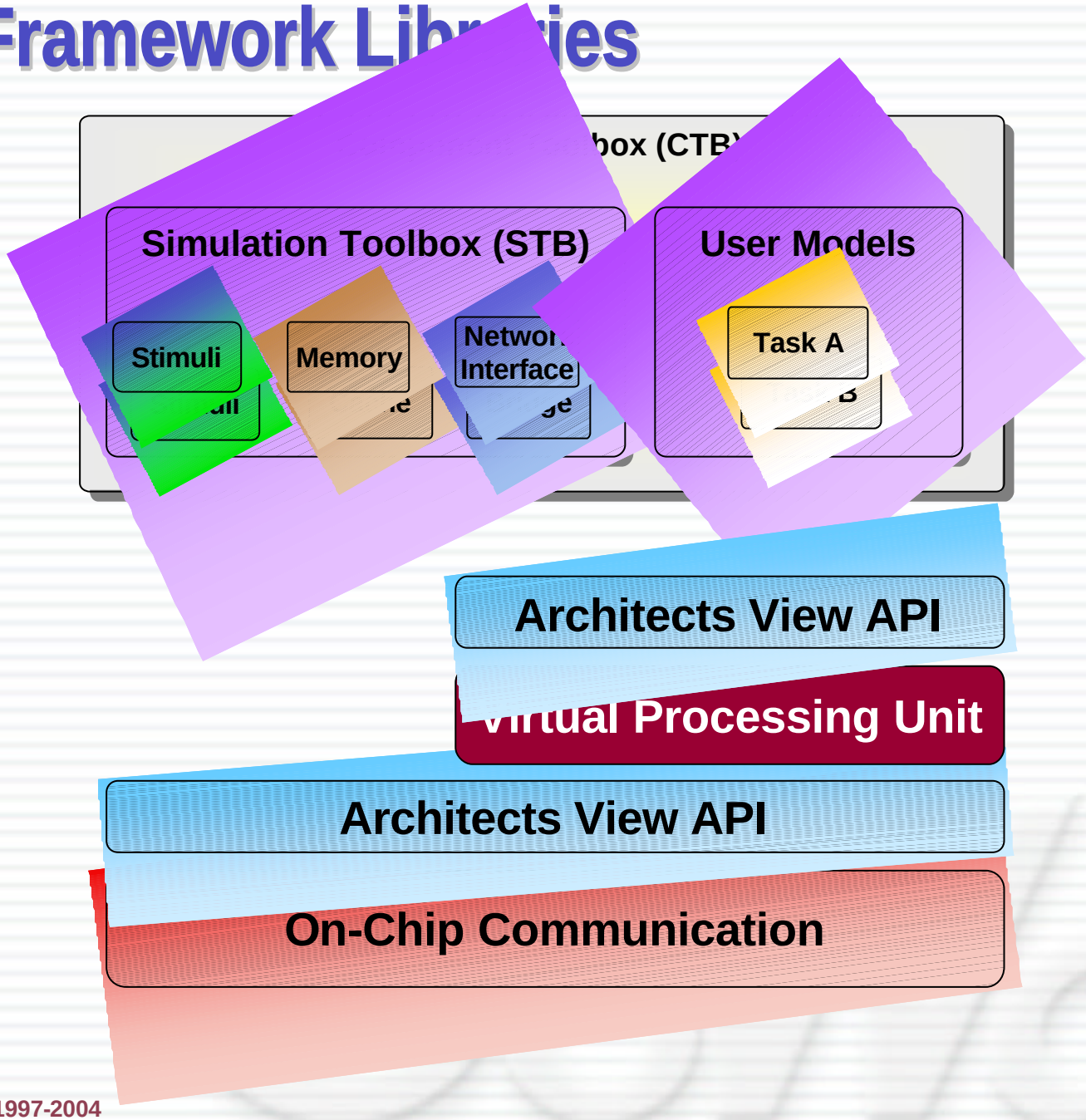
AV Framework Libr ies



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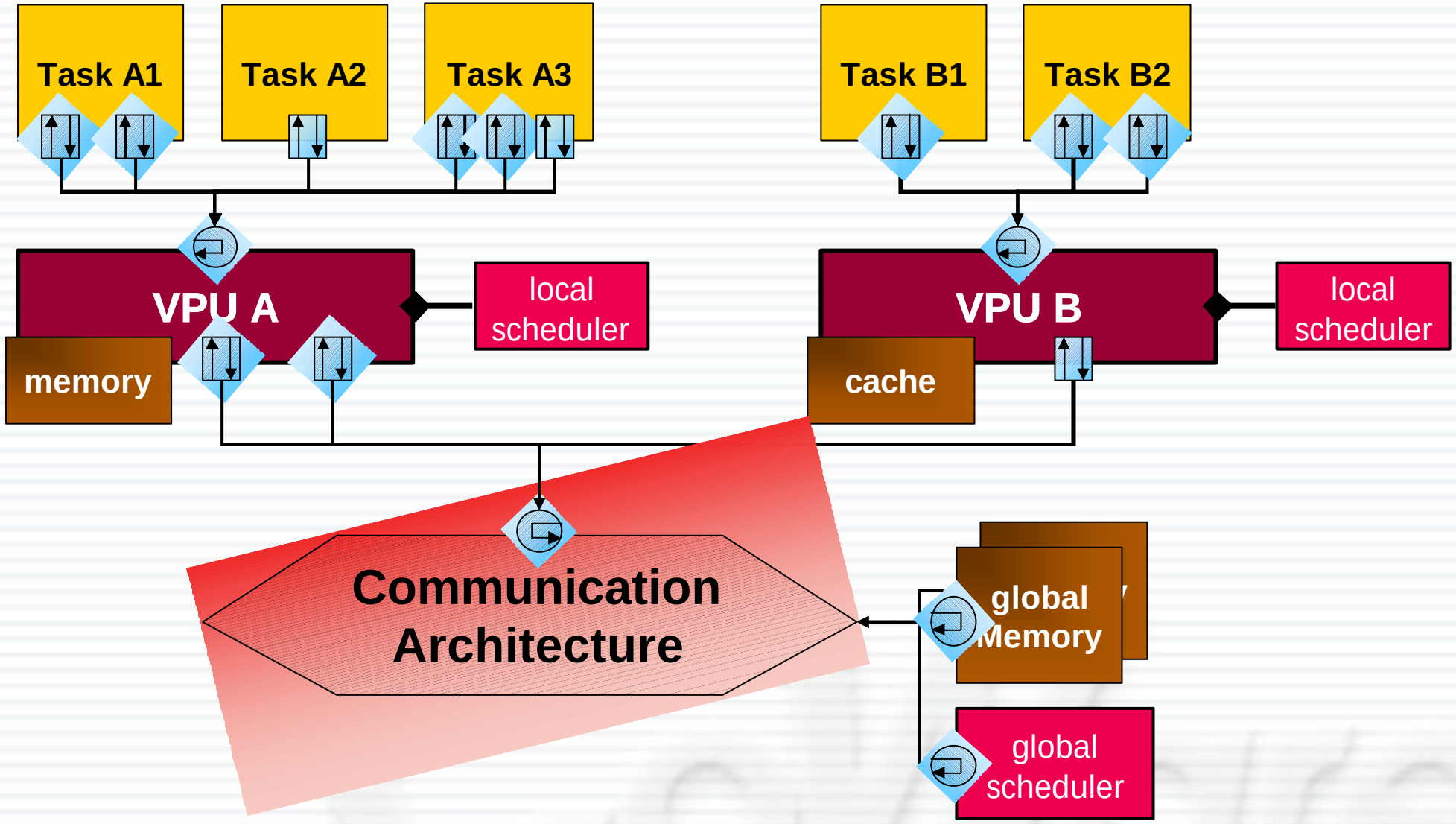
AV based Architecture Exploration and Partitioning



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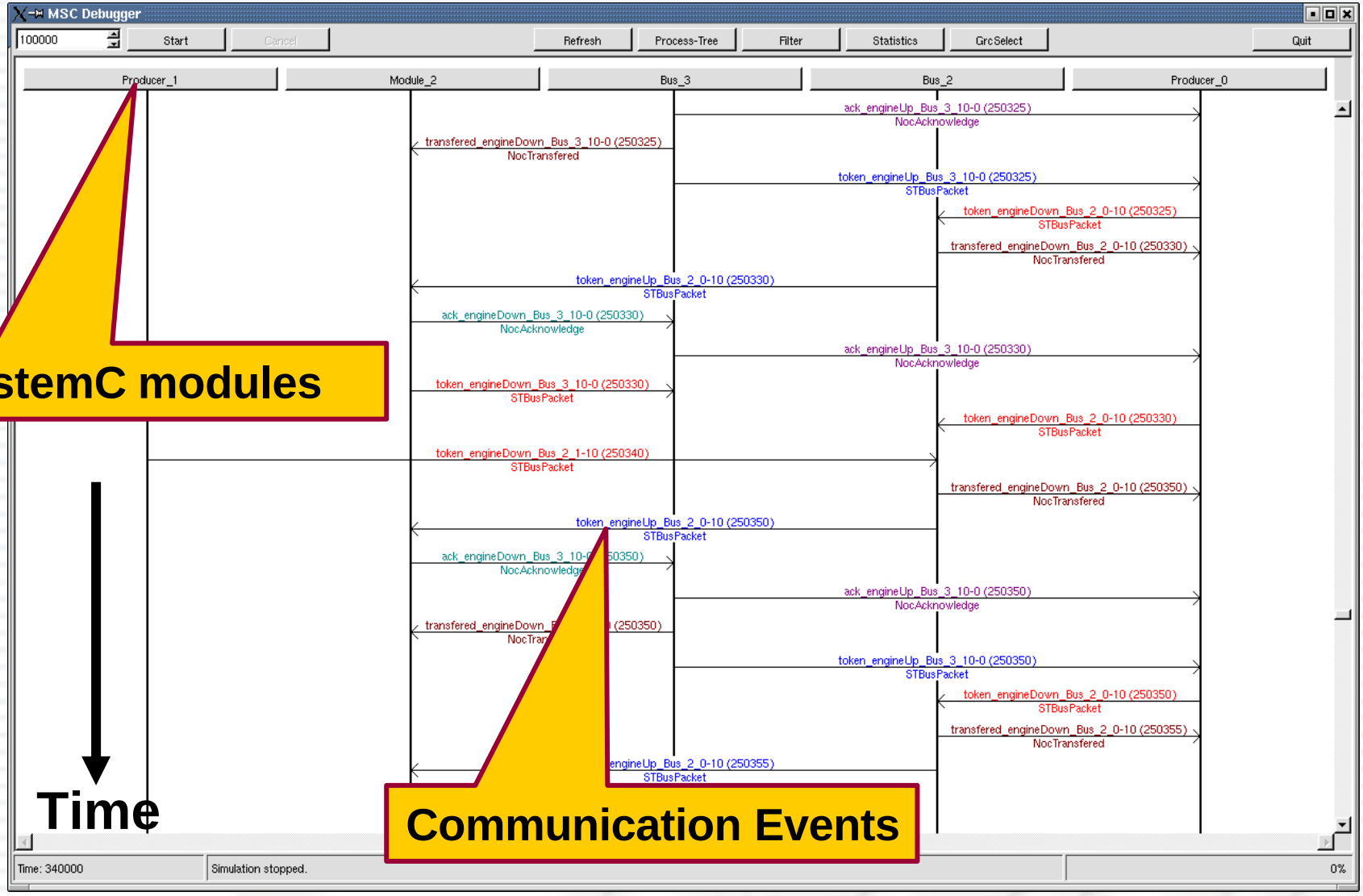
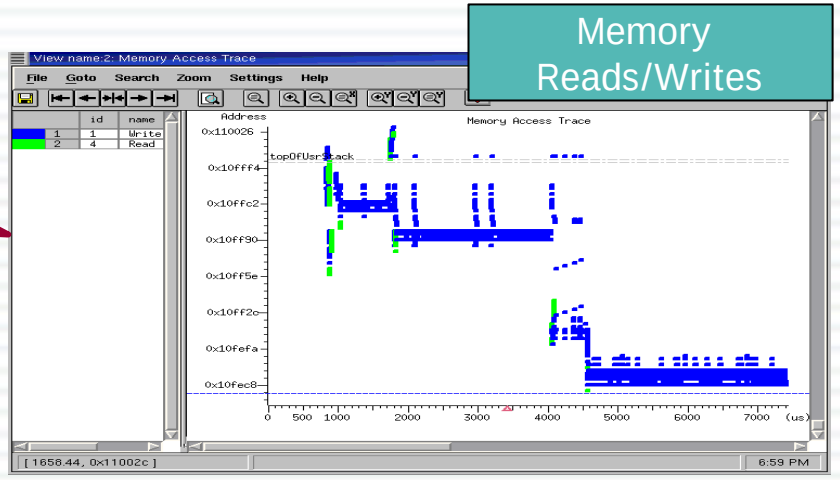
Message Sequence Chart Trace

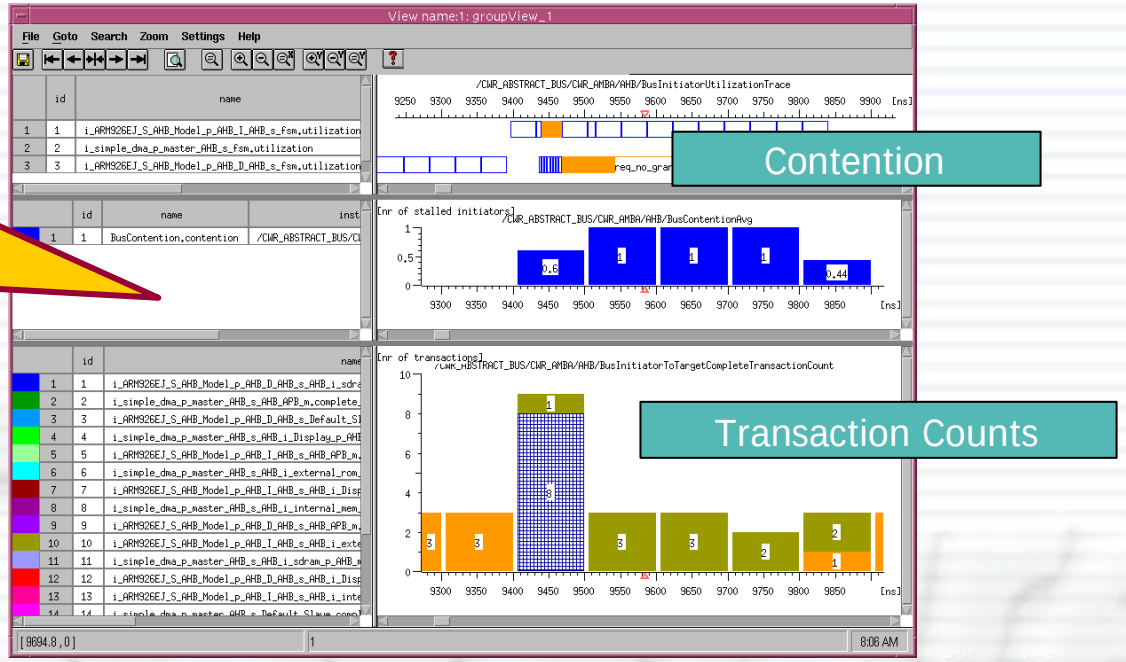


ConvergenSC Analysis

port/memory analysis
- **based on PlatformCreator address map**



bus analysis
- **all NoC nodes instrumented**
- **trace views**
- **statistical views**



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Summary

- Architects View Value Proposition
  - high abstraction level
    - simulation speed, modeling efficiency
  - generic synchronization protocol, declarative xml based configuration
    - modularity, flexibility
  - comprehensive set of debugging and analysis tools
  - scales to upcoming complexity challenges
    - Network-on-Chip
    - Multi-Processor SoC
  - OSCI TLM and OCP TL2 standard compliant
- Part of CoWare ConvergenSC Family
  - leverage Platform Creator, debugging, analysis, and fast simulator
  - seamless refinement to cycle-level TLM and RTL
  - IP library: processors, buses

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Thank You!

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