Open SystemC Initiative Briefing

Stuart Swan, OSCI Board Member

10th European SystemC Users Group Meeting

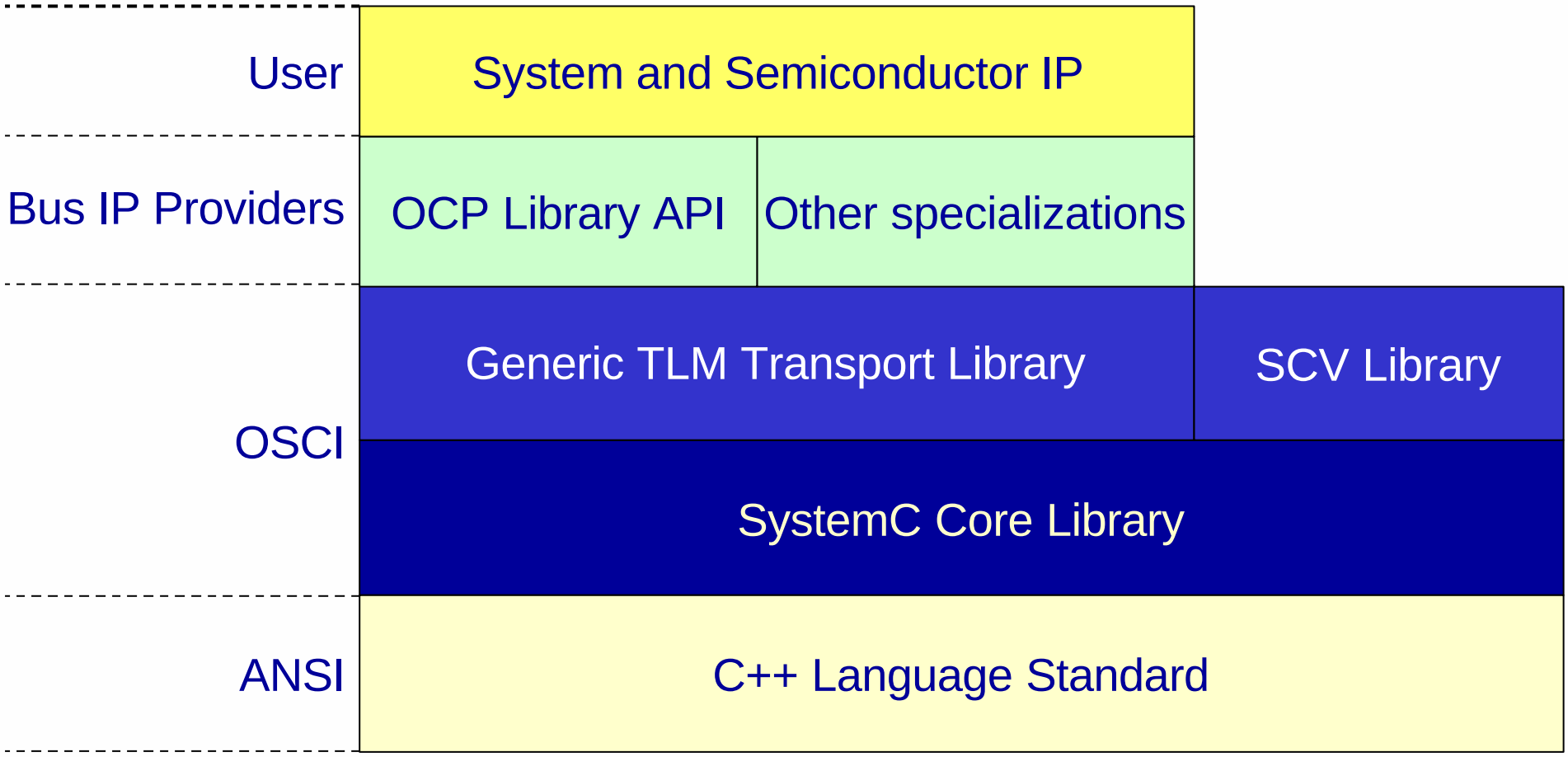
October 12, 2004

The Time for SystemC is Now!

- SystemC has emerged as the system-level standard
- Acknowledgement in the press
- Extensive use in industry
- Broad Commercial support

Isn’t it time you moved up to SystemC?

OSCI Layered Standards



Recent Press Coverage

According to Gary Smith there were 100 designs in 2003 using SystemC

Dr. Jack Horgan, EDA Weekly

The design of complex ASICs, application-specific standard products (ASSPs), and SoCs at the register-transfer level (RTL) is a dinosaur on its way to extinction.

. . .

With too much silicon area available to be filled and not enough time to fill it using the traditional flow, RTL is at the breaking point and the "design gap" we see in so many PowerPoint presentations is real.

David Maliniak, Electronic Design

If high-level co-verification is one driving force behind the re-emergence of ESL, SystemC is another.

Richard Goering, EEDesign

“SystemC is part of the reason that we're being able to move up [into higher levels of abstraction in design].”

Gary Smith as reported by Peggy Aycinena, EDA Weekly

Public Statements of Industrial Use

Semiconductor and Systems Companies

- Conexant
- Fujitsu Network Technologies
- Intel
- NEC Electronics
- Nokia
- Qualcomm
- Rohm
- Sony
- STMicroelectronics
- Texas Instruments
- Toshiba Semiconductor
- Toshiba Information Systems

Design and Verification Tool Providers

- Actis Design
- Adveda
- Aldec Inc
- Ascend Design Automation
- Axys Design
- Blue Pacific Computing
- Cadence Design Systems
- Celoxica
- ChipVision Design Systems
- CoFluent Design
- CoWare
- Dynalith
- EVE
- Forte Design Systems
- Mentor Graphics
- Prosilog
- SDV Inc
- Simucad
- Summit Design
- Synopsys
- Tenison EDA
- Verisity
- Veritools

Training and Consulting Providers

- Accel Technologies
- AmbLot SARL
- Blue Pacific Computing
- Cadence
- Doulos
- Eklectic Ally
- Forte Design Systems
- Fraunhofer IIS
- HDL Design House
- Hitachi Information Technology
- IMEC
- Lateral Sands
- Signa Technologies
- Synopsys
- Thinklake Design
- Transfer
- Willamette HDL

IP Providers

- ARM
- CoWare
- Endeavor Intertech
- HDL Design House
- SDV Inc
- Summit Design
- Synopsys
- TILAB SpA

The SystemC™ Community

- **Community Participants**
  - Semiconductor companies
  - IP companies
  - Systems companies
  - EDA companies
- **Licensees**
  - Free to all
    - Open source license
    - Download and use libraries
  - Participate in email forums
- **Members**
  - Participate in governance
  - Contribute to future direction
  - Participate in technical working groups
  - Have access to draft standards

OSCI Membership

- Corporate Members
  - ARM Ltd
  - Cadence Design Systems
  - CoWare
  - Forte Design Systems
  - Mentor Graphics
  - Synopsys
  - ST Microelectronics
- Associate Corporate Members
  - Calypto Design Systems
  - Celoxica Ltd
  - Eklectic Ally Inc
  - Fraunhofer Institute for Integrated Circuits
  - NEC Electronics America
  - Panasonic
  - Philips
  - Prosilog SA
  - SpiraTech Ltd.
  - Synfora Inc
  - Summit Design Inc
  - Tenison Technology EDA Ltd
  - Verisity Design Inc

Technical Working Group Activities

- **Language Working Group**
  - Developing core SystemC language
- **Verification Working Group**
  - Add-on libraries for verification
- **Synthesis Working Group**
  - Defining synthesizable subset of SystemC
- **Transaction Level Modeling Working Group**
  - Developing methodology and library for transaction-level communication

SystemC Language Reference Manual and IEEE Standardization of SystemC

- Enhancement of the SystemC LRM underway
  - Completed document describing 2.0.1 now being reviewed
  - Addition of 2.1 features planned to start immediately
- IEEE SystemC study group
  - Victor Berman Chairman
  - First meeting August 10
    - Discussed and approved a PAR
  - Next meeting planned for October

SYSTEMC™